Power Device Fabrication Using CMP

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Applications of CMP

- Classical microelectronics
  - Technology drivers: µ-processors, memory, ASICs, etc.
  - CMP: STI, replacement gates, ILD, W plugs, IMD, Cu metallization, TSV

- Micro-electro mechanical systems (MEMS)
  - Acceleration/angular-rate sensors, DLPs, MOEMS, RF-MEMS, micro machines
  - CMP: smoothing of poly-Si, planarization of sacrificial layers (metals, oxides, polymers), Cu-metallization

- New: Power devices
  - Power MOSFETs, super-junction FETs, "coolMOS", IGBTs
  - CMP: trench gates, W plugs, trench compensation structures, wafer thinning
Power Device Fabrication Using CMP: Outlook

- Power devices: power range and speed
- Power MOSFETs
  - Motivation: energy efficiency improvements
  - Basic structure of power MOSFETs
  - Trench power MOSFETs
  - Manufacturing steps - CMP
  - Super power MOSFETs: charge compensation structures - CMP
- IGBTs
  - Basic structure of IGBTs
  - Ultra-thin IGBTs: manufacturing steps - CMP
- Summary and Outlook
Power Devices

Wikipedia:
Power devices = semiconductor devices that are designed to handle significant power levels

Power MOSFETs

- Power MOSFET (Metal oxide semiconductor field-effect transistor)
  - Controlling or switching device for higher power levels
  - Up to several 100 A, up to 1000 V
  - In contrast to μA-mA range of CMOS devices

- Typical applications:
  - Switching power supplies
  - DC/AC converters for solar panels
  - Power management in portable computers, phones, MP3 players
  - Automotive (solid state relays, motor controllers, electric vehicles, hybrid cars)
  - Household appliances (e.g. induction heaters, regulated refrigeration)
  - Industrial electronics
  - Drives (frequency converters, e.g. in controllers)
Optimization of power MOSFETs

- Motivation: energy saving
  - World-wide electrical energy consumption
    2010 ~ 20,000 TWh
  - Server farms
    2010 ~ 200 TWh (~ 1 % of ww cons.) cooling: 50 %
    ⇔ 80 medium-size power plants (coal)

- Example: efficiency of switching mode power supplies
  Efficiency increase from 80 – 85 % in 2000
to 94 – 96 % in 2010
due to optimized circuit design and optimized power MOSFET devices
⇒ reduced heat production ⇒ reduced cooling ⇒ less CO₂
Power MOSFET

power MOSFETs have a vertical transistor structure! (3-dimensional device)

Typical technology:
CD = 0.35 – 1.0 µm
GOX = 15 – 100 nm
metal: Al, 2 – 5 µm thick
BS metal Ti/Ni/Ag
wafer size: 200 mm
Power MOSFET

„On“ state:
vertical current flow

Ideal device should have

- high conductivity
- fast switching
- small gate charge
- small capacities
Trench Power MOSFET

cell structure

power MOSFET = millions of paralleled transistor cells.
State-of-the-art:
giga-cells / inch$^2$
Trench Power MOSFET

Trench gate manufacturing steps:

- Trench etch (width ≈ 0.5 µm)
- Gate oxidation (10 … 100 nm)
- Poly-Si trench fill (n-doped)
- CMP of poly-Si

poly-Si CMP process:

- high selectivity to oxide ( >100 : 1)
- low dishing
Trench Power MOSFET

Contact and metallization manufacturing steps:

- Oxide dielectric & contact etch
- Ti/TiN sputtering & W CVD
- CMP of W

- high selectivity to Ti/TiN allows direct Al metallization

W CMP results: experimental slurry with 10 : 1 selectivity
High Voltage transistor: increase thickness of device!

Higher thickness of so-called drift zone leads to increase of $R_{DS(on)}$

largest impact has $R (n^{-}_{epi})$

Increase the number of charge carriers!

Drawback: reduction of blocking voltage
Introduction of vertical p-doped compensation structures allows higher doping of the voltage-sustaining $n_{\text{epi}}$-layer.
Super Junction Power MOSFET

„On“ state:
current flow

\[ n_{\text{epi}} \rightarrow n_{\text{epi}} \]

⇒ reduction of conduction losses by factor 5
Super Junction Power MOSFET

Reverse bias: formation of a pin-diode structure

increase of blocking voltage > 600 V
Super Junction Power MOSFET

Compensation structure manufacturing steps (before trench gate definition):

- Deep trench etch (d: 10 - 25 µm / w: 2 - 4 µm)
- Epitaxy trench fill (p-doped, B, $4 \times 10^{15}\text{cm}^{-3}$)
- CMP of Si
- CMP process: time-controlled or introduction of polish stop

non-selective or high-selective Si-CMP process solutions required
Power MOSFET with Fieldplate Compensation

Alternative:
fieldplate compensation instead of p-doped epitaxial compensation structures:
Power MOSFET with Fieldplate Compensation

Fieldplate compensation manufacturing steps:
- Deep trench etch
- Oxide filling: TEOS dep. 1.5 µm
- Deposition of poly-Si, n⁺ doped, 1 µm
- CMP of poly-Si, stop on oxide
- CMP of oxide (non-selective)
  → CMP problems: wafer bow due to layer strain
  → stress enineering
replacement of $n^+$ drain by p-doped emitter leads to gate-controlled pnp transistor

substrate thickness 70 µm (600 V)
IGBT (Insulated-Gate Bipolar Transistor)

Manufacturing steps:
- temporary bonding to handle wafer
- backside grinding
- smoothing and sub-surface damage removal: CMP of Si
- backside implant: n-field stop and p-emitter
- activation by annealing
- backside metallization

substrate thickness 70 µm (600 V)
Summary and Outlook

Summary

- Technology of power devices is several nodes behind state-of-the-art microelectronics
- CMP is employed since some years
- Increasing number of CMP applications
- Selective and unselective processes for poly-Si, W, oxide, c-Si, etc.
- Application-specific CMP slurries needed
- Examples shown are devices under development, not yet products
Summary and Outlook

Outlook

- New materials: copper, silicides
- New substrates: GaN, SiC
- Smaller structures: increasing application of CMP planarization
- Growing power devices market
  - ~ $23B in 2010 (~8% of semiconductor market)
  - annual growth rate ~ 7.5% in 2010 (iSuppli)
  - market share power MOSFETs ~ $6B
- IGBTs are used in hybrid / electric cars

from Wikipedia: Tesla Roadster
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