CMP for More Than Moore

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  • super powerMOS transistor
  • poly-Si angular rate sensor
  • infrared digital micromirror array
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ITRS 2007: additional non-digital functionalities incorporated into compact systems → “More Than Moore”
CMP for More Than Moore

More Than Moore
diversification

Analog/RF
amplifiers, SiGe, GaAs

Passives
“integrated discreetes”: R, C, L

HV / Power
IGBTs, powerMOS, (high V and/or high I)

Sensors / Actuators
MEMS: physical, opto, RF

Biochips
lab-on-a-chip, microarrays, nerve connections

→ “More Than Moore” is building upon microelectronics manufacturing technology
→ CMP is a key technology also for “More Than Moore”
## CMP for More Than Moore

### Comparison: CMP process requirements

“More Than Moore” vs. “More Moore”

<table>
<thead>
<tr>
<th>Category</th>
<th>More Than Moore</th>
<th>More Moore</th>
</tr>
</thead>
<tbody>
<tr>
<td>Larger structures</td>
<td>1 µm — 1 mm</td>
<td>dishing, erosion</td>
</tr>
<tr>
<td>Thicker layers</td>
<td>1 — 100 µm</td>
<td>higher RR, stress deformation</td>
</tr>
<tr>
<td>Planarity</td>
<td>relaxed / increased</td>
<td>e.g. optical flatness for mirrors</td>
</tr>
<tr>
<td>Layer materials</td>
<td>metals, polymers, ceramics</td>
<td>old/new slurries</td>
</tr>
<tr>
<td>Substrate size</td>
<td>100 — 200 mm</td>
<td>NU increased due to stiffer wafers</td>
</tr>
<tr>
<td>Substrate type</td>
<td>glass, ceramic, metal</td>
<td>fragility</td>
</tr>
<tr>
<td>Contamination</td>
<td>reduced req.</td>
<td>except: wafer bonding, powerMOS</td>
</tr>
<tr>
<td>Defects</td>
<td>reduced req.</td>
<td>micro roughness, scratches</td>
</tr>
<tr>
<td>Production</td>
<td>small unit numbers</td>
<td>throughput, reproducibility</td>
</tr>
</tbody>
</table>

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CMP for More Than Moore

Examples

case studies

- super powerMOS transistor
- poly-Si angular rate sensor
- infrared digital micromirror array
- capacitive RF-MEMS switch
Example: super powerMOS transistor

cross-section

Fieldplates for charge compensation:

- voltage range 80-400 V
- reduced on-resistance
  → high-power switch

1.5 µm TEOS
0.5 µm a-Si
15 µm trench depth
Example: super powerMOS transistor
trench fill and CMP

etch

1.5 µm TEOS

0.5 µm a-Si

CMP
**Example: super powerMOS transistor**

**CMP details**

<table>
<thead>
<tr>
<th>CMP Type</th>
<th>Slurry Type</th>
<th>Selectivity Requirements</th>
<th>Removal Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si polish</td>
<td>poly-Si slurry</td>
<td>high selectivity to TEOS</td>
<td>RR = 500 nm/min okay</td>
</tr>
<tr>
<td>TEOS polish</td>
<td>oxide slurry</td>
<td>standard fumed silica: low selectivity to Si</td>
<td>high removal rate (1.5 μm TEOS !)</td>
</tr>
</tbody>
</table>

required: high selectivity to Si

ceria slurry ?
Example: super powerMOS transistor

CMP details

Problem:
thick layers →
severe wafer bow (mm !)

TEOS: compressive stress
a-Si: tensile stress

additionally:
anisotropic stress due to
15 µm trenches

→ CMP non-uniformity
Examples

case studies

- super powerMOS transistor
- poly-Si angular rate sensor
- infrared digital micromirror array
- capacitive RF-MEMS switch
Example: poly-Si angular rate sensor
sensor device

Moving poly-Si comb (capacitor) structures for acceleration and angular rate sensors (gyros), height >10 µm, comb space 1 µm.

Coriolis-force angular rate sensor
Example: poly-Si angular rate sensor

rough Epi-poly

Epi-poly deposition: thick poly-Si (> 10 µm) layers show a rough surface ($R_a \approx 1$ µm) → litho problems → CMP
Example: poly-Si angular rate sensor
sensor fabrication sequence

- deposition of sacrificial oxide
- etching of anchor openings
- deposition of thick poly-Si (>10 µm)
- CMP of poly-Si
- etching of comb structures by DRIE
- etching of sacrificial oxide by vapour phase HF etch
Example: poly-Si angular rate sensor

CMP results

poly-Si CMP requirements
starting poly-Si thickness ≈ 14 µm
final poly-Si thickness = 11.35 µm
final poly-Si layer non-uniformity < ± 200 nm (range)

CMP process results
Cabot SS25 fumed silica based SiO₂ slurry removal Rate ≈ 0.5 µm/min
WIWNU < 2% (~55 nm (1 σ)) on 150 mm wafers
Rₐ ≈ 0.3 - 0.5 nm after Fujimi Glanzox buff

future: use of poly-Si slurry
Example: poly-Si angular rate sensor

gyro device

Sensor + ASIC in MCM:
signal range ± 300°/s
signal bandwidth 12 – 200 Hz

Applications:
vehicle dynamic control
car navigation
virtual reality

Development Partner:
SensorDynamics AG
Examples

Case Studies

- super powerMOS transistor
- poly-Si angular rate sensor
- infrared digital micromirror array
- capacitive RF-MEMS switch
Example: infrared digital micro mirror array
opto-MEMS device

256 x 256 pixel micro-mirror array for infrared imaging system
Example: infrared digital micro mirror array cross-section

CMP 3: Cu sacrificial layer
~ 10 µm thickness
stop on Ni posts

CMP 2: Cu damascene incl.
TaN barrier

CMP 1: Oxide planarization
of CMOS passivation

3 CMP steps needed in the fabrication sequence
Example: infrared digital micro mirror array

CMP results: thick Cu polishing (CMP 3)

Cu-CMP slurry: commercial product with inherently high selectivity to Nickel (Cabot iCue® 5003) on IC1000 k-grv.

- Removal rate > 0.5 µm/min
- Polishing time > 5 min, in-situ conditioning
- Roughness $R_a < 3$ nm

high selectivity to Nickel posts achieved

dishing between Nickel posts < 100 nm for mirrors 80 x 80 µm size

→ sufficiently flat for IR applications
 CMP for More Than Moore

Example: infrared digital micro mirror array
final device

Mirror array with tilted mirror after CMP 3
and copper sacrificial layer etch
Examples

case studies

• super powerMOS transistor
• poly-Si angular rate sensor
• infrared digital micromirror array
• capacitive RF-MEMS switch
Example: capacitive RF-MEMS switch

schematic 3D-view of capacitive switch

20 GHz capacitive RF-MEMS switch
Example: capacitive RF-MEMS switch manufacturing flow

CMP of Cu sacrificial layer

1. Ti/Pt/Au/Pt stack
2. dielectric 1
3. Cu-
4. Au/ Ni/Au membrane
5. CMP with Au lines
6. thick Ni anchoring
7. Final layer
Example: capacitive RF-MEMS switch
Cu sacrificial layer thickness optimization

final Cu sacrif.-layer thickness: 2.85 \( \mu m \)

which Cu starting thickness is required for a planarity < 50 nm?

1 \( \mu m \) pattern height reduction depending on
• polishing time (removal)
• consumables set (pad, slurry)

\( \rightarrow \) Cu start thickness: 4.5 \( \mu m \)

1.65 \( \mu m \) Cu to be removed by CMP
Example: capacitive RF-MEMS switch
evolution of planarity (Cu-slurry 2 / pad B)

- Unpolished: pattern height 1000 nm
- 0.64 µm mean removal: pattern height 346 nm
- 1.51 µm mean removal: pattern height 17 nm

Ra (plane) = 2.0 nm

Micromap 512 white-light interferometer
Further examples
application of CMP for “More than Moore” microsystems

Wafer bonding
- Si-CMP for direct wafer bonding
- oxide CMP for anodic bonding
- grinding/polishing of glass frit for “laser soldering”
  (encapsulation of micro sensors)

Backside CMP
- grinding/polishing of Si
  - replacement of double-side polished wafers
  - ultra-thin silicon: stress relief after grinding

3D integration (TSVs)
- metal CMP for removal of material overburden
Future developments

Other layer materials  SiC, Si$_3$N$_4$, SiGe, Ge, Ni, Au, diamond (CMPable?)

Other substrate materials  glass, ceramics, metals, polymers

Damascene scheme  alternative for structuring of materials

New applications  piezo materials (e.g. PZT) for actuators
LEDs, displays, photovoltaic
heat dissipation (smooth surfaces)

Thank You