Notable Trends in CMP: Past, Present and Future

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Pete Singer
Editor-in-Chief

Levitronix CMP Users’ Conference 2007
April 1988: Etchback, SOG

Techniques for Planarizing Device Topography

Planarization of device topography becomes increasingly important as geometries approach 1 μm. Many techniques are available to planarize, each with its own advantages and disadvantages.

Kathy Slusser, Associate Editor

Device planarization, the reduction of vertical height for enhancement process sizes below 1 μm, is necessary as geometries begin to shrink. Planarization is most often during the backend process where intermetallic and dielectric layers are used. It is much easier to image fine-line geometries on wafer planes, hence the need to planarize. Growth into a film of the mask does not create uniform topography.

The main techniques available for planarizing cover surfaces can be divided into two types: dielectric planarization and metal planarization. Dielectric planarization involves removal of all conductor raised steps and formation of new raised steps on the surface lines. Metal planarization requires filling up or planarization of the lines.

Dielectric planarization

Dielectric planarization — one of the two main types — involves the smoothing of an insulating film in an IC device. The second type of accomplishing this task will be discussed.

Thermal flow

Dielectric thermal flow is used to smooth precursor topography. The temperature of the substrate is raised to the point where it will flow, smoothing over the steps below it (Fig. 1). This can be accomplished either by raising the wafer temperature to a level above the softening point of the insulating film or by using a low-pressure thermal annealing equipment. Dielectrics typically used are pure SiO2 and phosphorus pentoxide (P5O5) doped SiO2, deposited by chemical vapor deposition (CVD).

Thermal flows, however, do not flow to the high pressure typically used in other applications (Fig. 2) to avoid cr knapping. The deposition equipment used to apply thermal flows should be designed to allow substrate temperatures to be reduced to levels acceptable for use over continuous substrates, such as wafers, and on multi-substrate systems, films that can withstand higher temperatures. Flow temperatures are reduced by using a lower ambient. BiFlow, a commercially available source of SiO2, can be reduced from the softening point of pure SiO2 to under 800°C.

Excimer lasers can be used to planarize metal films using flow techniques. (Source: KBR Inc.)
Planarizing Leading Edge Devices

Chip makers are looking to integrated processing and chemical-mechanical polish to planarize their advanced devices.

Victor Corsello, Associate Editor

This dielectric layers are placed on top of each other until the spaces are completely filled. In this sandwich-like layers of CFAB (illicite) glass with layers of silicon nitride (SOG). The top surface of the layers is then polished to create an etch-back with a photomask.

Spin-on glass

As its name implies, a spin-on glass dielectric is spun on a wafer as a liquid and then cured at a high temperature, similar to the SOG glass (silicon oxynitride) that is easily formed. This type has the advantages of flexibility and high density. This film of the glass material is spun onto the wafer, the layers are then baked, and the glass is then coated onto the wafer. There are two techniques used: "spin-on" and "spin-coating." These techniques are used to spin the glass film onto the wafer.

1. Phosphosilicate: SOG left over metal lines where etch will not be used. (source: Metacodes Inc.)

2. Single-coat polyimide layer across 4, the Polyimide test module. (source: Du Pont Electronics.)
March 1992: Local vs Global

Searching for Perfect Planarity

As depth of focus shrinks below 1 μm in today's lithography tools, planarity becomes critical at all device levels.

Peter R. Hage, Senior Editor

What do silicon wafers and glass cocktails doped in white chocolate have in common? Not much, says semiconductor executive D. Francisco (Frans) van der Wiel, who recently received the ACES 1992 award for his contribution to the semiconductor industry. Yet the two have something in common. According to van der Wiel, "When I look at a wafer, I see the planarity of the wafer was totally predetermined by the chocolate." He remembers.

By comparison, Dr. Herbert — and hundreds of others like him around the world — have to work very hard to totally planarize the rough irregularities of a silicon wafer. Dr. Herbert, and those used to achieving higher levels of planarization include polishing the front-face of the wafer with an abrasive chemical slurry, sputtering it with a layer that bonds it to a glass wafer, and then polishing it with a smooth, glass wafer. The result is a wafer that is perfectly flat.

Clearly, the need for these and other kinds of planarization techniques (which is increasingly more of a problem) is driven by the need to control the cost of planarization. According to van der Wiel, "When we can achieve 1 μm in lithography, we can reduce the number of masks needed to perform lithography on a wafer. This is because lithography plays an integral role in the wafer's planarity and can be improved by planarization techniques. The result is a wafer that is perfectly flat.

Global vs local planarization

Perhaps not surprisingly, the same drives to smaller dimensions that make lithography more challenging also make it more critical to achieve truly global planarization. The result is a wafer that is perfectly flat.
February 1994: Pads and Slurries

Chemical-mechanical Polishing: A New Focus on Consumables

Research is now targeted on ways to better understand and control the subtle interactions between the wafer, pad, and slurry.

Pete Singer
Senior Editor

Key Technologies:
- Planarization
- Chemical-mechanical Polishing
- Polishing Pads & Slurries

At a Glance:

Two things appear to be certain about chemical-mechanical polishing: The first is that it's absolutely essential, and the second is that it's far from perfect. It's estimated that some 40 percent of all wafers are rejected because of non-uniformity, which is too high for the industry to ignore. The challenge is to find a way to improve the process and make it more efficient.

To address these challenges, SEMI (the Semiconductor Equipment and Materials International) has launched an initiative called the Chemical-mechanical Polishing Technology Task Force. The goal of the task force is to bring together experts from around the world to develop a better understanding of the process and to identify areas for improvement.

The task force is made up of representatives from companies such as IBM, Intel, Motorola, IBM, and others. They are working on various aspects of the process, from the design of the polishing pads to the development of new slurry formulations.

One of the main challenges is to find a way to control the polishing process more precisely. This involves understanding the interactions between the pad, slurry, and wafer, and how these interactions affect the final surface quality.

The task force is also looking at ways to improve the efficiency of the process, such as reducing the amount of slurry used and minimizing the amount of time the wafer needs to spend on the pad.

Another area of focus is the development of new polishing technologies, such as the use of diamond-like carbon (DLC) pads. These pads are more durable and can withstand higher pressures than traditional polishing pads.

Overall, the task force is making significant progress in improving the chemical-mechanical polishing process. With continued research and development, we can expect to see even better results in the years to come.
Chemical-Mechanical Polishing of Dual Damascene Aluminum Interconnect Structures

A new study shows it is possible to minimize dishing and scratches on aluminum surfaces while achieving high selectivity and good electrical yield.

**Effects of Slow Removal Rate (Center Foot)

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<tr>
<th>Process</th>
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**Chemical-Mechanical Polishing of Dual Damascene Aluminum Interconnect Structures**

Chemical-Mechanical Polishing (CMP) has been used in IC production since the mid-1980s, with many variations of the process evolving over time. In this study, a new polishing technique has been developed that minimizes dishing and scratches on aluminum surfaces, achieving high selectivity and good electrical yield.

**Key Technologies:**
- **Planarization**
- **Aluminum deposition**
- **Chemical-mechanical polishing**

**Results:**
- The new polishing technique reduces dishing and scratches on aluminum surfaces, improving the selectivity and electrical yield.
- The technique is particularly effective in applications requiring high electrical yield and minimal dishing, such as interconnect structures in advanced ICs.

**Comparison with Traditional Techniques:**
- Traditional polishing techniques often result in excessive dishing and scratches, especially on high-aspect-ratio structures.
- The new technique minimizes these issues, leading to improved electrical performance and yield.

**Conclusion:**
- The new polishing technique represents a significant advancement in IC fabrication, enabling higher yield and better electrical performance.

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**Table 1: CMP Process Parameters**

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<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Polishing pressure</td>
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<tr>
<td>Polishing speed</td>
<td>x.xx m/min</td>
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<tr>
<td>Etching rate</td>
<td>x.xx m/min</td>
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<tr>
<td>Selectivity</td>
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**Notes:**
- The values in Table 1 are indicative and may vary based on specific process conditions.
- Further research is ongoing to optimize these parameters for different IC applications.

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**Figure 2: Typical SEM micrograph of planarized AI damascene architecture.**

The new polishing technique results in a smooth, flat surface with minimal dishing, facilitating better electrical performance and yield.

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**Figure 3: Typical SEM micrograph of local post-CMP damascene structure.**

The polished surface shows minimal dishing and scratches, ensuring high-quality electrical connections.

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**Figure 4: SEM micrograph of representative post-CMP bond pad and surface.**

The polished bond pad shows a smooth, consistent surface, ideal for high-quality bonding and electrical connections.

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**References:**
November 1994: Cu and Low k

New Interconnect Materials: Chasing the Promise of Faster Chips

Copper and low-k dielectrics have the potential to reduce RC time delays and boost chip speed.

Semi-conductor manufacturers are facing a major problem: how to reduce the resistance of the copper interconnects, which are typically 300-400 ohms. One approach is to use a composite dielectric material in the interconnects, which not only reduces the resistance of the copper, but also reduces the dielectric constant of the interconnects. This approach has been used in some circuit designs, but it has not been widely adopted due to concerns about reliability and scalability.

Another approach is to use low-k dielectrics, which have a lower dielectric constant than traditional silicon dioxide. This reduces the capacitance of the interconnects, which in turn reduces the delay time.

Copper is a good conductor, but it has a higher resistance than aluminum. It is also more difficult to etch, which can lead to manufacturing difficulties. Low-k dielectrics are also more difficult to process, which can lead to reliability issues.

Despite these challenges, low-k dielectrics are being used in some high-performance circuit designs. They are expected to become more common in the future as manufacturers continue to push for faster chip performance.

Program in copper: In addition to low resistances, copper has several other important advantages. It can be deposited using chemical vapor deposition (CVD), which is a more efficient and less expensive process than the traditional sputtering process used for aluminum. Copper is also more resistant to electromigration, which can cause metal lines to grow and eventually break down.

In conclusion, low-k dielectrics and copper interconnects have the potential to significantly improve the performance of future chips. While there are challenges to overcome, these materials are expected to play a key role in the development of high-performance computing and other applications.
Albany Nanotech Today
November 1995: Maturation

CMP: Suppliers Integrating, Applications Spreading

With greater process knowledge emerging, chemical mechanical polishing is poised to move into a wider range of applications.

Pieter Buijsmaat
Senior Editor

Key Technologies:
- Chemical mechanical polishing
- Wafer planarization
- Process integration

At A Glance:
Increasingly out of the expensive, esoteric process it was originally, chemical mechanical polishing (CMP) is on the verge of an explosion in applications. First, we are seeing a rapidly growing list of suppliers for this technology. Currently, only a handful of suppliers are showing an unusual degree of partner activity and cooperation to bring process control to what has been a process art. Second, while CMP was originally a process for expensive microprocessor production by major IC manufacturers who could support the costs, now CMP is useful for an ever-widening array of products, from modern chips to wheels. Third, there are a number of new markets for CMP, such as silicon-on-insulator, wafer fabrication, and multiprocessor module assembly. The future promises to bring integrated systems, possibly even integration with chemical vapor deposition systems, and an all-inclusive CMP cost of ownership.

Chemical mechanical polishing (CMP) has been in production since the mid-1980s. The process originated, closely guarded, when IBM and Intel first worked together on microprocessor development and production. "In those days, it was called 'wafer planarization,'" says X-ray (Raninda) Pui, director of process technology at IBM. "We had a two-layer process, but that's all we knew." The world was ready for a new approach, and CMP was the answer.

"As wafer sizes increased and thickness decreased, the vertical polish was important," Pui explains. "And the surface quality was terrible. The dimples would cause problems in the oxide." CMP, which uses a polishing agent, polish pad, and water slurry, serves to polish the oxide to a smooth, planar surface. The result is a significantly better surface than a wafer planarized with a CMP technique. "We need a very smooth surface, and chemical mechanical polishing appears to be the answer," Pui says.

"By the mid-1980s, IBM and IBM suppliers were spending a lot of money on CMP," says Ken McCall, a senior engineer at IBM. "We were devoting a lot of resources to this process. We still are.

But as CMP technology matured, it became clear that it might have a future in other areas. Today, CMP is used in a variety of applications, from microprocessor fabrication to silicon-on-insulator, wafer fabrication, and multiprocessor module assembly. The future promises to bring integrated systems, possibly even integration with chemical vapor deposition systems, and an all-inclusive CMP cost of ownership.

Process details missing

Despite the long history, process details are still sketchy. Companies who have been doing CMP for a long time protect process secrets very closely. Pui explained, "We will not tell customers who commercially available carrier films they use, or whether they use organic or inorganic polishing powders. While much of the technology is proprietary, we can say that CMP technology has matured.

"It has been a barrier to entry for other semiconductor manufacturers getting into CMP. Now, CMP is on the cusp of being commercialized, perhaps even entering the mainstream. The technology is nearing the point where it can be used in a variety of applications. CMP technology is ready to take off."
Empirical data indicates fracture toughness below 0.3 MPa-m^1/2 is problematic for CMP stacks and back-end packaging (wire bonding).

* Trademark of The Dow Chemical Company
2002: Endpoint enhances Copper CMP Process Control

Stages of Copper polish:
(for edge thin Cu deposition or edge-fast Cu CMP removal)

- Pre-CMP
- Copper Planarized
- Edge clearing first
- Center last to clear
- Copper cleared to barrier

### Topography:

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- **Dishing minimized with FullScan + Non-Selective slurry**
Advantages of Cu ECMD Technology
2004: CMP Failure Model Analysis for Cu/ULK Integration

Mechanical Strength

Deformation = \( C \frac{F_{sc}}{W^3 H} \)

Line Width

- 180 nm: 1049
- 130 nm: 285
- 100 nm: 100
- 70 nm: 24
- 50 nm: 6
- 35 nm: 1.5

ACM Research, Inc.
2004: DFM Optimization

Step 1: Copper Plating

Step 2: Bulk Polish

Step 3: Copper Clear or Touchdown

Step 4: Barrier Removal

Source: Pregasus
Ecmp Planarization Solution

Ecmp is Planarization and Process Control by Charge

**CMP**
- Good planarization
- Down force dependent
- Large feature dishing, Dense array erosion
- High cost

**EP**
- Conformal removal
- Down force independent
- Excessive dishing, Minimum erosion
- Low cost

**Ecmp**
- Superior planarization
- Down force independent
- Minimum large feature dishing, Minimum erosion
- Low cost

Possible damage to fragile low-k films
November 2004: Slurry Pumping

Effect of Shear Stress and Pump Methods on CMP Slurry

Conventional wisdom suggests that shear stresses generated by centrifugal pumps are too high to allow use of the pumps for delivery of shear-sensitive slurries. This article shows that a shear-optimized centrifugal pump can circulate slurry with minimal damage, compared with tradition slurry delivery methods. Formation of large particles, which can cause water defects and can limit the life of system filters, was significantly less with a centrifugal pump.

At a Glance

The large particle, considered to be particles >6.3 μm in diameter, cause surface roughness during planarization. Furthermore, an increase in the concentration of large particles may prematurely plug filters, thereby reducing their lifetime and increasing maintenance costs.

Results and discussion

Figure 1 shows the effect of shear stress concentration on the PSD of the working particles. Data are shown for both the mean particle diameter (volume weighted) and for 99% permeable particle diameter (i.e., particle size greater than the 99% permeable particle diameter). The permeable particle diameter typically ranges from 100 to 200 nm. The data shown are averages of five measurements. No significant change in mean particle size or 99% permeable particle diameter was observed with any pump after the chip was tested over 1000 times.

Changes in the cumulative concentration of large particles as a function of particle diameter for each pump type are shown in Figure 2. Each curve represents the PSD after a given number of tests between 0 and 1000 tests. The concentration of large particles (>20 μm) increased significantly within 1000 tests. However, no significant difference was seen between the slurries pumped or the centrifugal or diaphragm pumps. After 1000 tests, concentrations increased to 20-25 times higher than the initial concentration, depending on the particle size. 

The centrifugal pump system, large particle concentrations remained relatively unchanged. The particle concentration increase was observed to be essentially linear with no evidence of the formation of large particles in the low pump.

These results suggest that these pumps generate a consistent flow of large particles per headset stroke, ~200000 for 16” and 144” diaphragm pumps. Since the pump delivers a constant volume per stroke, this is equivalent to a constant increase in the mean particle size. This is consistent with a linear increase in the cumulative distribution of large particles.
June 2005: Low-k Damage

Damage Mechanisms in Porous Low-k Integration

As a Glance

The effects of different etch times or etch-to-undertop ratios. All samples received the same hardmask prior to etch followed by a wick etch. The CMP/PRM (a) and (b) show the damage to the (a) and (b) planes to the depth-to-surface ratio of 3:1. The damage to the (a) and (b) planes to the depth-to-surface ratios of 3:1. The damage to the (a) and (b) planes to the depth-to-surface ratios of 3:1.

DAMAGE MECHANISMS IN POROUS LOW-k INTEGRATION

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Effect of Polymer on Ash Damage

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Delineation with Staining

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Text Structure

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As a Glance

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High-Retention Filtration of CMP Slurries

The specifications for chemical mechanical polishing (CMP) processes are becoming more complex and demanding as new devices are manufactured with new materials on larger wafers. As a result, the improved planarity and lower defect levels have resulted in the use of the working particles in CMP slurry being reduced. More filtration to remove unwanted large particles while maintaining the required working particle size distribution (PSD) is critical to the CMP process quality. Most CMP slurries now use 10-50 nm particles at typical concentrations of 1-30 wt% solids. Such small particles have resulted in increasing demand for high-accuracy, low-cost 0.3, 0.5, and 0.8-μm filters with substantial large particle removal and high-retention performance for any given slurry. This is critical to filtration technologies, especially since the difference in size between the particles to be retained and those to be passed through is less than one order of magnitude. For filtration, submicron CMP particles, deep media made from submicron (fume) materials are used. Performance is strongly dependent on the distribution of these sizes and the arrangement of the filters within the medias. Filters with small particles provide better retention and lower drop characteristics than larger fibers, but a proper balance between the sizes is needed for optimal filter performance for any specific slurry.

As a Glance

1.5 and 0.5 μm med filters demonstrate superior filter characteristics for use as point-of-use and distribution loop filters for silicon slurry. Also, the importance of carrier fiber selection is demonstrated.

Placing filters further improves the large particle retention. Depth media can also be graded, placing more open layers at the filter inlet and tighter layers towards the outlet (Figure 1). Filter design complexity is increased by the presence of fibers in some slurries. To remove solids effectively without dramatic reduction in filter lifetime requires a large 3D structure that allows gas capture through the depth of the finest open media layers. Gas capture just on the top surface of the thicker media will widely lead to flow reduction and blocking. Formation of this base often leads to media compression and a significant increase in resistance as well as pressure drop. Silica-based fibers show a particular requirement for evaluation of the fibers with various length. When the length of the filter, position of the fibers, and length fibers. At the same time, such filters must have reasonable high-flow rates and long lifetime.

We have developed filters using the above design guidelines that meet the most demanding CMP slurry filtration requirements. This paper demonstrates the availability of filters for such processing duties at the particle collection (PDC) and in the distribution loop. We also highlight the importance of empirical verification of a filter’s performance with particular slurries as part of filter selection. Results from filtration studies of slurries for oxide (silica fiber), silicon nitride (silica + carbon) and copper (alumina fiber) CMP as well as polycrystalline (PCE) head challenge solutions are presented and show that retention, flow rates, and pressure drop characteristics have very different behaviors for the varying processing conditions. This verifies that CMP slurries are critical filter selection criteria. We also show that graded filters with fibers are effective in managing large particles in CMP slurries.

Methodology

A silica-based fiber (Silica x) with <2 μm solids was evaluated to generate filter retention and pressure drop data for typical CMP slurries. At a typical concentration of 20-30% solids, the filter effectiveness was measured at various filter sizes using a particle size analyzer (PSA) aimed at 0.3, 0.5, and 0.8-μm particles. In some cases, there are different ways of characterizing the retention curve. By using multiple layers of the same media, the required smaller particle size can be reduced, while simultaneously reducing the whole particle filter size. In other cases, the large particles will experience an increasing particle retention to a higher retention. This behavior is more evident when being reconfigured through the 0.8-μm deep media. The global flows and pressure drop performance was evaluated by measuring the LPC and APD in the filter. Shown is Shunt LPC and Pressure Drop (Pd) for the different slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A second set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

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A twelfth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A thirteenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A fourteenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A fifteenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A sixteenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A seventeenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A eighteenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A nineteenth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].

A twentieth set of experiments was conducted to obtain filter retention, flow rate, and pressure drop data for various CMP slurries. All slurries and slurries used in this study. The flow-through reconstituted slurries from the above tests were also measured in single point tests using high-speed shear: 90, 150, 200, and 300% [SD].
### Cu/Low-k Integration Issues that Impact Performance and Reliability

<table>
<thead>
<tr>
<th>Issue</th>
<th>Tradeoffs</th>
<th>Example</th>
<th>This Work</th>
<th>∆C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polish stop</td>
<td>TDDB, erosion vs. C</td>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
<td>-10%</td>
</tr>
<tr>
<td>Etch stop</td>
<td>Rs tolerance</td>
<td><img src="image3.png" alt="Diagram" /></td>
<td><img src="image4.png" alt="Diagram" /></td>
<td>-10%</td>
</tr>
<tr>
<td>Cap thickness, k</td>
<td>E-M, T/C, via-yields vs. C</td>
<td><img src="image5.png" alt="Diagram" /></td>
<td><img src="image6.png" alt="Diagram" /></td>
<td>-10%</td>
</tr>
<tr>
<td>SiCOH damage</td>
<td>S-M, E-M, CD, strip vs. C</td>
<td><img src="image7.png" alt="Diagram" /></td>
<td><img src="image8.png" alt="Diagram" /></td>
<td>-5%</td>
</tr>
<tr>
<td>CD control</td>
<td>TDDB, RIE/strip vs. C</td>
<td><img src="image9.png" alt="Diagram" /></td>
<td><img src="image10.png" alt="Diagram" /></td>
<td>-15%</td>
</tr>
<tr>
<td>Via heights</td>
<td>T/C, yields vs. C</td>
<td><img src="image11.png" alt="Diagram" /></td>
<td><img src="image12.png" alt="Diagram" /></td>
<td>-5%</td>
</tr>
</tbody>
</table>


- The challenge: retain a manufacturable process with minimal capacitance and maximal reliability
- No poisoning, plasma damage, CMP damage, residual moisture, CD control problems, defects, etc.
November 2006: Outsourcing

Outsourcing CMP
Process Development and Materials Evaluations

By outsourcing CMP capability, Freescale accelerated engineering evaluations and kept internal resources focused on production demands.


The semiconductor industry’s recent upturn is driving higher fab utilizations and requiring fabs to maximize the effective use of their resources. This, in turn, drives the need for additional projects to allow for increased production and cost savings. These types of projects are typically focused on improving process yields, reducing cycle time in a fab’s tool operations, reducing consumption of consumables, or enhancing new methods for either improved performance or reduced costs. Unfortunately, fabs’ resources are often consumed in projects because of the increased demand for production resources. This leaves the ability to execute vital engineering projects just when these projects would have the greatest impact.

One solution to increasing production output & conserving its focus on production is to identify additional work capacities. Consequently referred to as the “Black Box” or “Brown Box” model, this solution allows companies to increase work targets beyond their internal capacity limits during periods of high demand while decreasing the risks of carrying out these cap save during periods of work demand. While this solution may be well suited for companies needing additional fab-wide capacity, a more flexible and dynamic option is preferred for addressing constraints in specific process modules.

As one of the newer and faster growing processes in a modern fab, the chemical-mechanical planarization (CMP) process module is frequently one of the processes subject to capacity constraints. It is also often targeted for cost reductions and productivity improvements. In order to address these issues and minimize the impact on manufacturing production, Freescale Semiconductor elected to outsource certain engineering projects for CMP material evaluations and process improvements to Fremoce, a dedicated CMP foundry. By doing so, Freescale was able to focus limited resources on immediate production success while still addressing the improvement projects in a timely fashion with external resources. This article reviews the initial results of these efforts and describes the synergistic benefits that Fremoce was able to achieve by leveraging expertise for specialized semiconductor CMP services.

A novel approach

It is outsourcing of CMP material development work, ongoing for one fab! The simple answer is leverage. By leveraging the available resources and CMP expertise of an external service provider, the fab is able to keep internal CMP resources more tightly focused on production requirements and still execute engineering projects in parallel. The external company provides the technical staff, time on process tools, and metrology for data collection to ensure at least a portion of the engineering projects that might otherwise compete with available production resources in the fab. The table shows a comparison of approaches resources base to create a typical CMP experiment requiring three days of polishing time by two different pads over using externally sourced lab expertise and the other showing lab workweek of the same experiment executed by an outsourcing provider.

Removal Rate and Uniformity Comparisons

November 2006 – SEMICONDUCTOR International 45

- Guide CMP ‘normal’ sets and uniformly for a development polishing set.

- Normal Total CMP ‘normal’ set and uniformly for a development polishing set.

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Critical Factors for Any CMP Process

• Wafer / Materials Parameters
  – Size / Shape / Flatness
  – Film Stack Composition
    • Metals (Al, Cu, W, Pt, etc.)
    • Oxide (TEOS, PSG, BPSG, etc.)
    • Other (polysilicon, low-k polymers, etc.)
  – Film Quality Issues
    • Stress (compressive or tensile)
    • Inclusions and other defects
    • Doping or contaminant levels
  – Final Surface Requirements
    • Ultralow surface roughness
    • Extreme planarization, esp. Copper
    • Low defectivity at <0.12 um defect size

• Pad Issues
  – Materials (polyurethane, felt, foam, etc.)
  – Properties must be chosen for the job
  – Conditioning method often not optimized
  – Lot-to-lot consistency

• Slurry Issues
  – Chemistry optimization often required
  – Mixing and associated inconsistency
  – Shelf life and pot life sometimes very short
  – Slurry distribution system (design, cost, upkeep)
    • Agglomeration and gel formation
    • Filtration is often required
  – Cleaning method specific to slurry and film
  – Waste disposal and local regulations

• Process Issues
  – Long list of significant input variables
    • Downforce
    • Platen speed
    • Carrier speed
    • Slurry flow
    • Conditioning method
      – Disk used (material, diamond size, spacing, etc)
      – Force
      – Speed
      – Sweep profile
  – Highly sensitive to local pattern variation
  – Must maintain consistency at high throughput
  – Must optimize for variation of incoming films

• Integration Issues
  – Materials Compatibility
    • Electrochemical interactions with two or more metals
    • Film integrity and delamination, esp. low-k
    • Film stack compressibility
  – Interactions with adjacent process modules
    • Photolithography
    • Metal deposition and metal etch
    • Dielectric deposition and etch
  – Electrical design interactions
    • Feature size constraints
    • Interactions with local pattern density
    • Line resistance variation, esp. damascene copper
    • Dielectric thickness variation
    • Contact resistance variation

Development and manufacturing teams must achieve technical performance requirements while balancing complexity, cost, risk and timelines.
The Future

Thank You!