PRODUCTION OF ULTRA-FLAT SEMICONDUCTOR WAFER SUBSTRATES USING ADVANCED OPTICAL LENS POLISHING TECHNOLOGY

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Outline

- Flatness measurement data
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ABSTRACT

Semiconductor materials are used in a wide variety of devices such as field effect transistors (MosFets, Fets), integrated circuits (ICs, MMICs, ASICs), focal plane arrays, infra-red detectors, and other novel devices. Silicon is common for many device applications. Achieving flatness of silicon wafer substrates is becoming increasingly important in the sub-45 nanometer gate length regime. The semiconductor Fabs have little or no capabilities to polish wafers below total thickness variation (TTV) value of 1.0 micron. However, ASML-Optics has extensive experience in producing ultra-flat optical lens surfaces which is directly applicable to polishing of ultra-flat wafers. This technical paper will describe existing in-house capabilities of chemi-mechanical polishing (CMP) operation at ASML-Optics and demonstrate its ability to produce ultra-flat wafers. Detailed thickness as well as flatness uniformity data is presented for CMP processing of 200-mm diameter silicon wafer substrates. Our advanced lens polishing technology employs patented CMP operation to produce ultra-flat surfaces. The ultra-clean polishing slurries are utilized in order to provide extremely flat surfaces with very low levels of trace metals. Our advanced CMP process can be tailored to provide ultra-flat wafers needed for advanced silicon-on-silicon and silicon-on-insulator thermal bonding technology which is employed for fabrication of MEMS devices. This unique CMP technology can also be effectively adapted for compound semiconductors, most commonly used are gallium arsenide, silicon carbide, indium phosphide, cadmium sulfide and cadmium telluride. The computer controlled polishing tool can be useful in producing ultra-flat thickness calibration standards needed for metrology systems. Our state-of-art metrology tools have a capability to generate a detailed pixel-by-pixel map of peak-to-valley (PV) flatness values and LPD's counts up to 300-mm diameter wafer substrates.

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OBJECTIVES

- Introduce ASML proprietary optical lens polishing process

- To present technical data for production of 200-mm semiconductor wafers with total thickness variation (TTV) less than 0.5 micron.

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METRICS OF INTEREST

- Peak-to-valley (PV)
- Total thickness variation, TTV (GBIR),
- Bow-3pt,
- Warp-bf

*GBIR = Global back ideal reference

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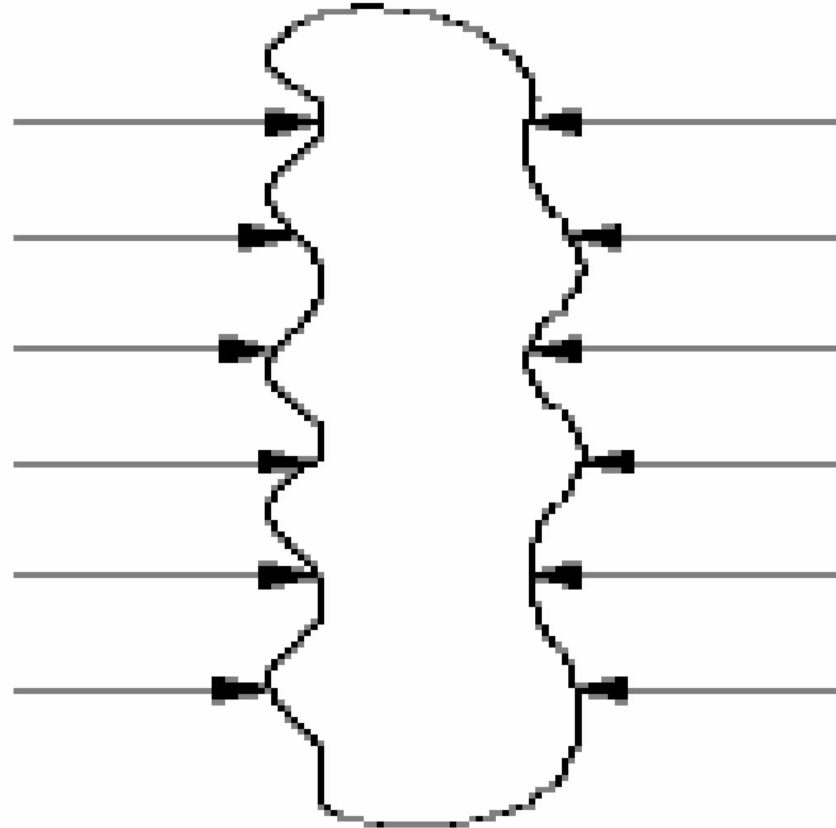
MEASUREMENT THEORY (TTV MEASUREMENTS)

- **Thickness measurements** - the distance through the wafer between corresponding points on the front and back surfaces
- **Total Thickness Variation (TTV)** - the difference between the maximum and minimum values of the thickness of the wafer.



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TTV VS. PV

- **Total thickness variation (TTV):** TTV is based on front and back measurements of a wafer and is dependent upon thickness of the wafer.

- **Peak-to-valley (PV):** PV is only front based and it is independent of wafer thickness.

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COMPARISON OF POLISHED WAFER FLATNESS AND THICKNESS UNIFORMITY DATA

(200-MM DIAMETER SILICON WAFER)

Wafer Slot #	Zygo Interferometer	ADE Model # 9700 Gage (16K POINTS & EE = 2 MM)			ADE Model # 9700 Gage (16K POINTS & EE = 5 MM)			ADE Model # 9900 Gage (32K POINTS & EE = 5 MM)		
	PV, µm	TTV, µm	Warp-bf, µm	Bow-3pt, µm	**TTV, µm	Warp-bf, µm	Bow-3pt, µm	TTV, µm	Warp-bf µm	Bow-3pt, µm
2 (Pre-CMP)	1.411	6.74	11.16	1.99	6.81 ± 0.004	10.40	2.22	8.25	7.87	4.21
1	0.179	2.76	3.54	2.34	2.00 ± 0.010	3.54	2.47	2.09	5.31	3.13
3	*TBM	3.94	9.78	-3.98	2.32 ± 0.010	8.76	-3.22	2.54	8.33	0.03
4	0.095	1.77	9.73	4.55	1.26 ± 0.007	9.49	4.85	1.36	9.20	5.41

*TBM = To be measured.

** Represents mean value ± one standard deviation of ten measurements taken on wafers.

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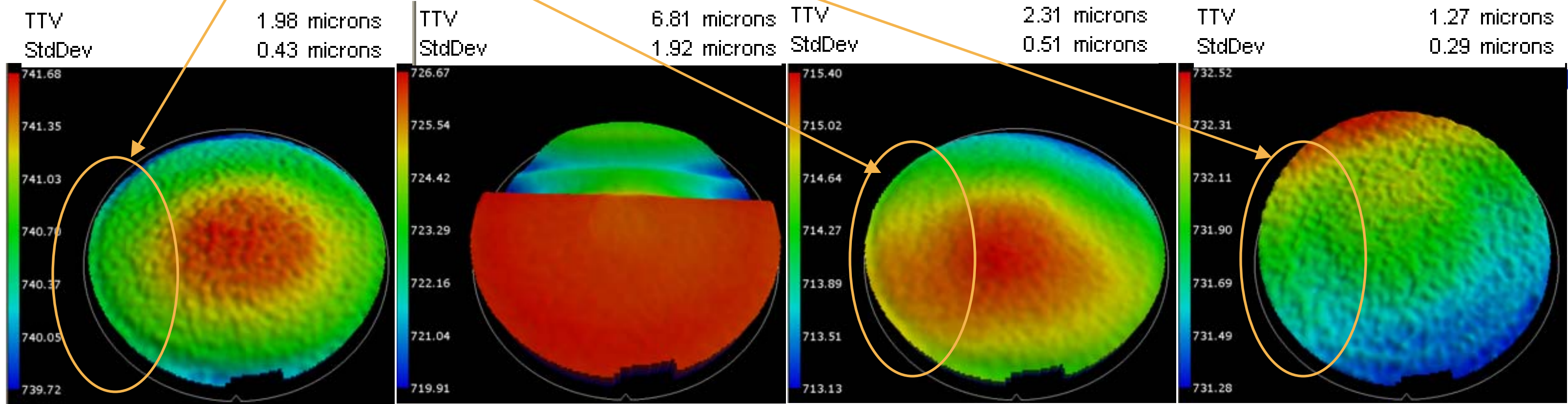
POST-CMP DATA (16,000 POINTS & 5-MM EDGE EXCLUSION

Edge ring on slots 1 and 3, but not on 4

Wafer Slot	1	2	3	4

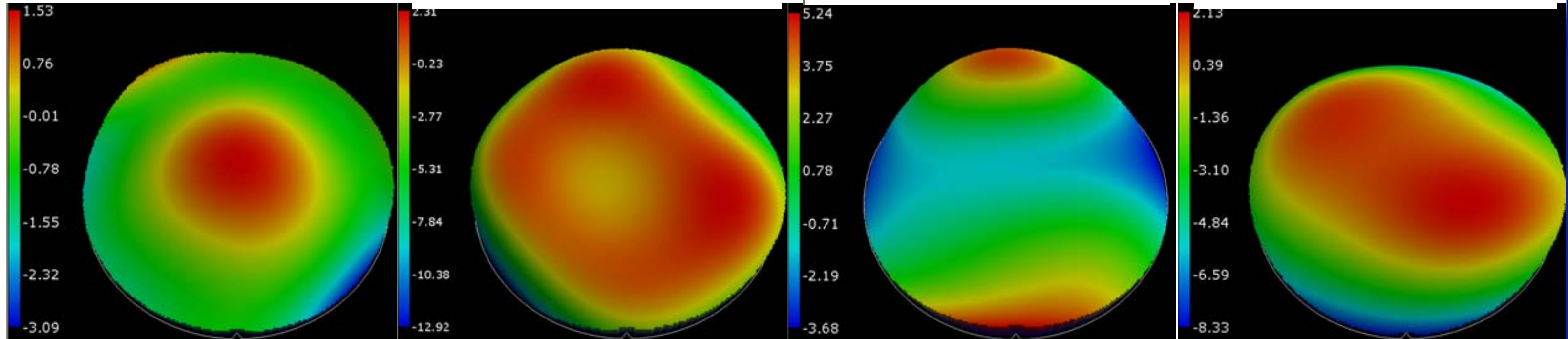
Thickness

	1	2	3	4
TTV	1.98 microns	6.81 microns	2.31 microns	1.27 microns
StdDev	0.43 microns	1.92 microns	0.51 microns	0.29 microns



Shape

	1	2	3	4
Bow (bf)	1.28 microns	-1.18 microns	-2.08 microns	1.24 microns
Warp (bf)	3.54 microns	10.61 microns	8.63 microns	9.35 microns
Min Warp (bf)	-2.24 microns	-8.24 microns	-3.41 microns	-7.17 microns
Max Warp (bf)	1.30 microns	2.37 microns	5.22 microns	2.18 microns



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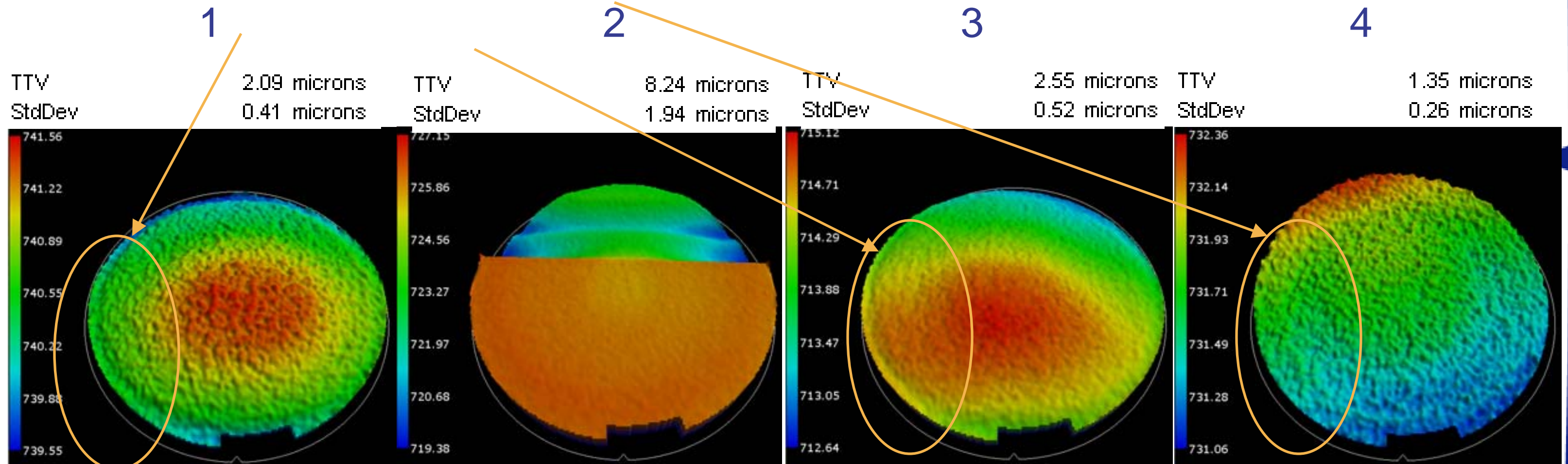
POST-CMP DATA
(32,000 POINTS & 5-MM EDGE EXCLUSION

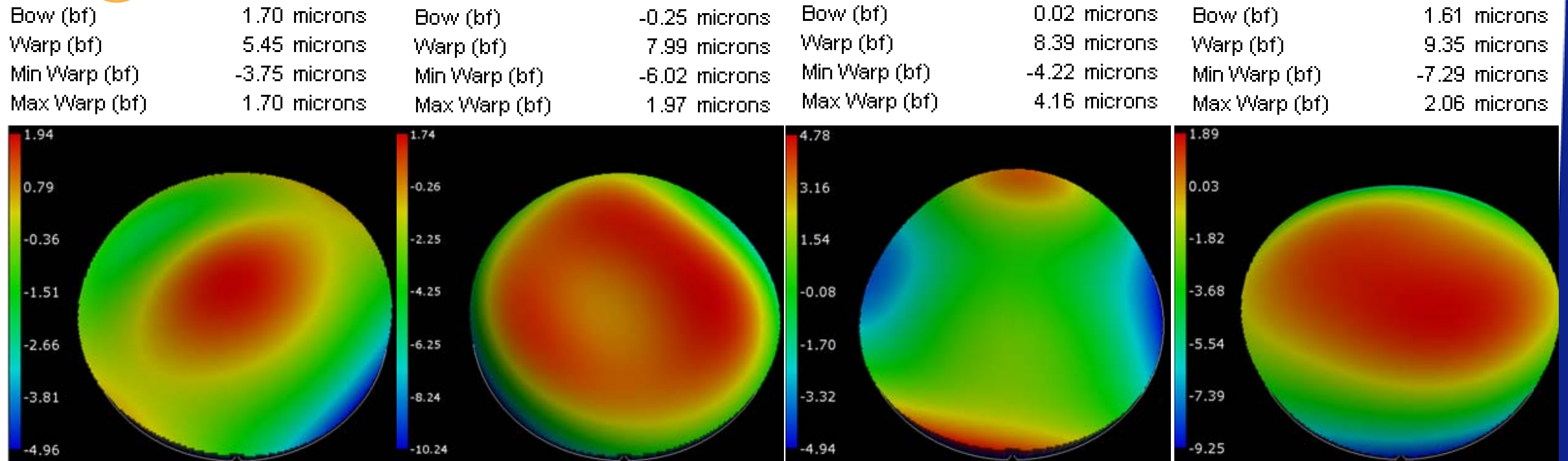
Increased spatial resolution of 9900 provides more clarity of edge ring

Wafer Slot

Thickness



Shape



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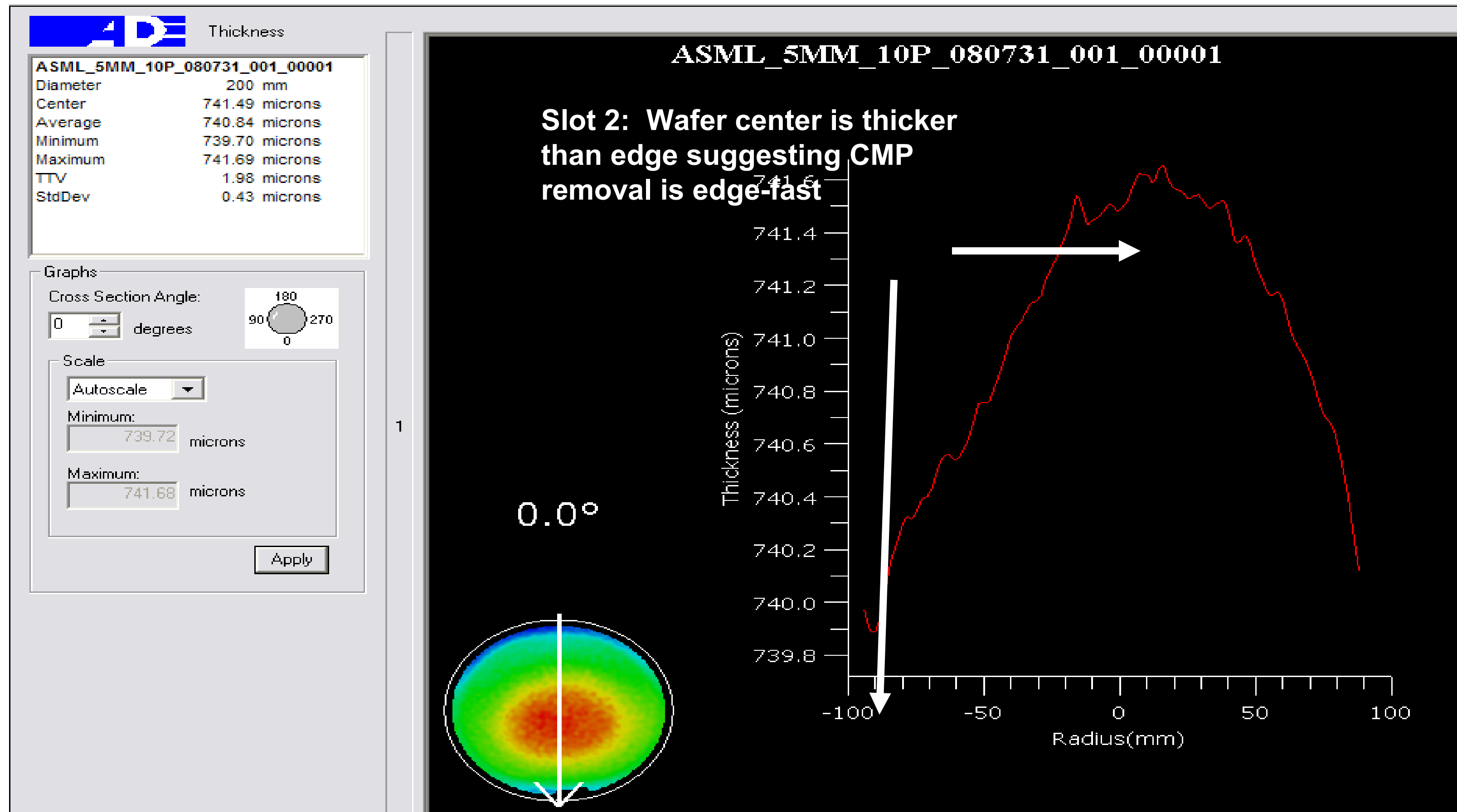
CROSS-SECTION ANALYSIS



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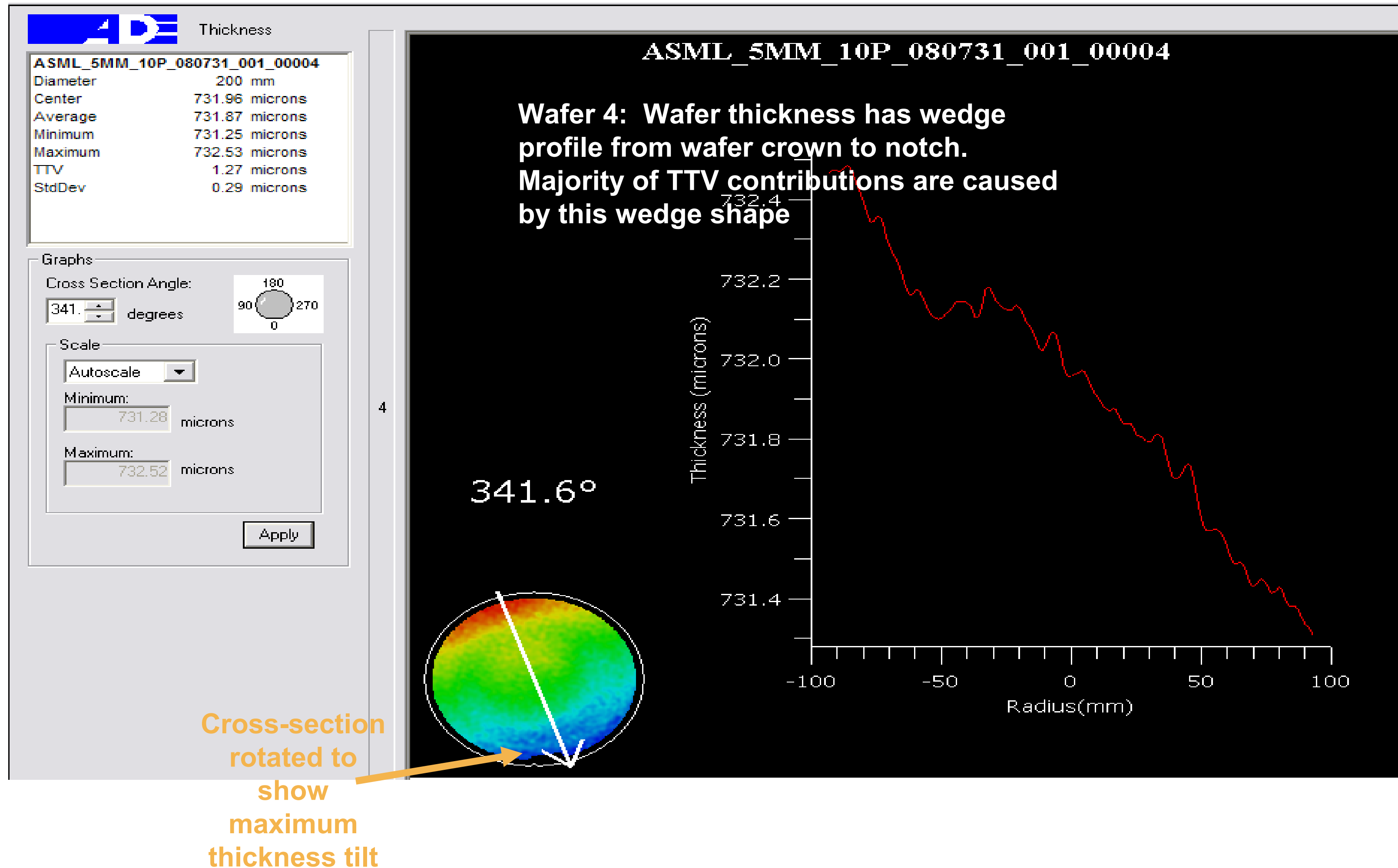
CROSS-SECTION ANALYSIS (Cont.)



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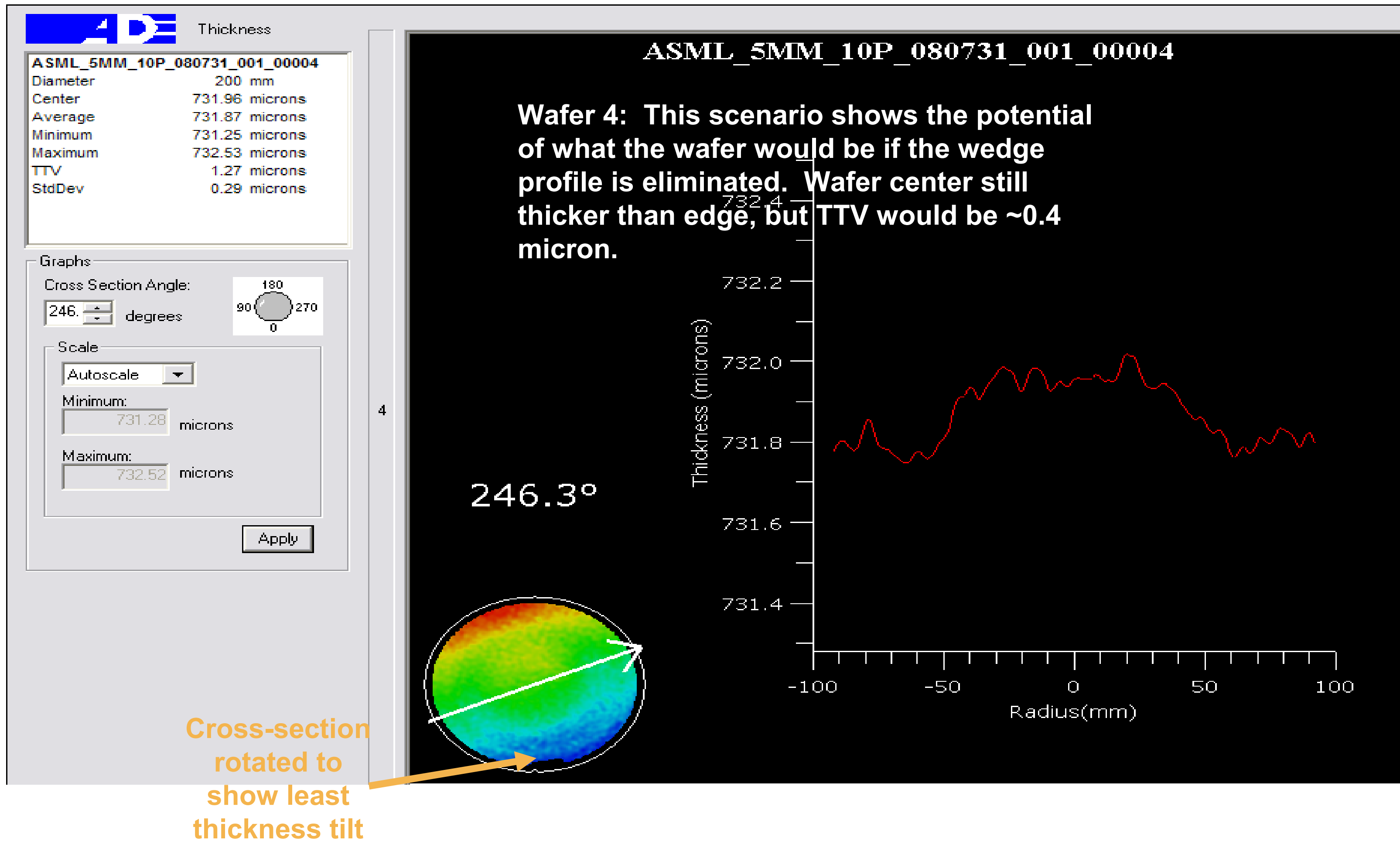
CROSS-SECTION ANALYSIS (Cont.)



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CONCLUSIONS

- TTV, Bow, and Warp metrics were analyzed using two different mapping systems.

- Slot # 2 wafer TTV contribution was mostly affected by having a faster edge removal criterion.

- Slot # 4 wafer had the best TTV.

- TTV contribution in slot # 4 was mostly caused by wafer thickness tilt.

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CONCLUSIONS

- Thickness map cross-section analysis show that slot # 4 has a thickness tilt that has the most effect on TTV.

- Slot # 4 TTV was measured at about 0.4 micron when wedge profile was eliminated.

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KEY BENEFITS

- Precision polishing process
- Extremely suited for optical substrates
- Adaptable for custom semiconductor bare silicon and process substrates
- Capability of providing surface accuracies of 1/20-[lambda] P-V and, with more care, can achieve 1/50-[lambda] P-V or better surfaces.

CUSTOMER COLLABORATION

ASML is interested in collaboration with an external IC customer and semiconductor fab in this proprietary optical lens polishing technology for providing ultra-flat silicon wafers.

Thank You

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